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### REMARKS

Applicant concurrently files herewith an Excess Claim Fee Payment Letter and fee for excess claims.

Claims 1-9 and 21-33 are all the claims presently pending in the application. New claims 21-33 have been added to more completely define the invention.

It is noted that the claims have been amended solely to more particularly point out Applicant's invention for the Examiner, and not for distinguishing over the prior art, narrowing the claim in view of the prior art, or for statutory requirements directed to patentability.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "Version with markings to show changes made".

Claims 1-6 and 9 stand rejected under 35 U.S.C. §102(b) as being anticipated by Sasaki et al (JP 09-145965) (hereinafter "Sasaki").

Claims 1 and 6-8 are rejected under 35 U.S.C. §102(b) as being anticipated by Tada (U.S. Patent No. 5,684,902) (hereinafter "Tada").

These rejections are respectfully traversed in view of the discussion below.

### I. THE CLAIMED INVENTION

Applicant's invention, as defined for example in independent claim 1 is directed to a semiconductor laser diode chip and a method for mounting the chip onto a substrate.

A feature of the present invention includes first and second measurement marks at positions relative to an active layer which are used to correctly position the chip with relation to the active layer and the measurement marks.

With such features, it is possible to accurately position an LD chip to a substrate using a passive alignment technique even when there have been errors in a production process (e.g. see page 4, lines 9-12 and page 5, lines 1-13).

An exemplary configuration of the inventive structure is shown in Figs. 3 and 8 of the application.

The conventional structures, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and fail to provide for such

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advantages.

Indeed, such features are clearly not taught or suggested by the cited references.

## II. THE PRIOR ART REFERENCES

The Examiner asserts that:

*[regarding claims 1-6 and 9] Sasaki et al. discloses the claimed invention. Figure 1 illustrates a semiconductor laser chip comprising a first mark, a second mark...*

*[regarding claims 1 and 6-8] Tada et al discloses the claimed invention. Figure 3a-3c illustrates a semiconductor laser chip comprising a first mark and a second mark.*

However, Applicant respectfully disagrees.

The present invention, as defined by independent claim 1, and as shown for example in Figs. 3 and 8 of the invention, is directed to a semiconductor laser chip 20 to be applied to an optical module. The laser chip 20 (e.g., as shown in Figure 3; all reference numerals used here are for the Examiner's clarity and understanding for exemplary purposes only and not for limiting the claims in any way) of the present invention has two types of marks to perform a positioning operation. Position marks are for making a position adjustment between a position of the laser chip and a position of the substrate arranged with an optical fiber. For example, as shown in Fig. 8, the position operation is performed by adjusting the position marks 35, 36 on the laser chip to align with position marks 44, 45 on the surface of the substrate 40.

The measurement marks 17, 18 as shown in Fig. 3 of the present invention, are located near the active layer 11 to correct a position between an active layer 11 and measurement marks 15, 16. In the case that a position between both active layer 11 and measurement marks 15, 16 is accurate, the active layer 11 of the laser chip can be made exactly at a position on the substrate 40.

However, in the case where a position between both active layer 11 and measurement marks 15, 16 is not accurate, the active layer 11 cannot be made exactly at a desired position to the optical fiber. The position aberration occurs while forming the active layer 11 and the marks 15, 16 in the masking process. Thus, it is possible to obtain accurate positioning

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operation by measuring the distance between the active layer and the second marks 17,18.

In sharp and fundamental contrast, Figure 1 of Sasaki discloses first marks 5 formed on a laser semiconductor laser chip and second marks 14 formed on a substrate 10. However, unlike the present invention, Sasaki's semiconductor laser chip only has one type of marks on the chip itself. Thus, Sasaki fails to disclose measurement marks formed on the chip to correct a distance between an active layer 6 and first marks 5.

That is, Sasaki's chip cannot be accurately adjusted to the substrate 10, especially where there is a position aberration between an active layer 6 and the (first) position marks 5. Therefore, Sasaki clearly differs from the present invention and fails to anticipate or render obvious the claimed invention.

Tada is no more relevant than Sasaki. Tada also discloses two kinds of marks. However, as shown in Fig. 3(a) of Tada, the laser chip 3 does not have measurement marks like those of the claimed invention. Instead, the laser chip of Tada only has markers 19 on the chip which (arguendo) correspond most closely with position markers 15, 16 of the invention. Thus, Tada also does not teach or suggest the measurement marks on the chip of the present invention including "*a second mark that satisfies a predetermined relative position relation to said first mark and is positioned oppositely to a substrate-side mark formed on said substrate*". Therefore, the structure of Tada is clearly different from that of the present invention and does not anticipate or for that matter render obvious the claimed invention.

Thus, Applicant submits that the present invention is clearly distinguished from the system disclosed in Sasaki and Tada.

Hence, turning to the clear language of independent claim 1, there is no teaching or suggestion of "*[a] semiconductor laser diode chip comprising:*

*a first mark formed at a predetermined position with respect to an active layer on a face opposed to a substrate to which the chip is mounted; and*

*a second mark that satisfies a predetermined relative position relation to said first mark and is positioned oppositely to a substrate-side mark formed on said substrate at mounting time to said substrate*" (emphasis Applicant's).

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, dependent claims 2-9 when combined with independent claim 1 define additional novel and non-obvious features.

Additionally, new independent claims 21 and 31 (and dependent claims 22-30 and 32-

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33) have substantially similar novel and non-obvious features.

Also, the other prior art of record has been reviewed, but it too even in combination with Sasaki and Tada fails to teach or suggest the claimed invention.

### III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-9 and 21-33, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

  
Sean M. McGinn, Esq.  
Reg. No. 34,386

# 46,060

Date: 4/17/02

McGinn & Gibb, PLLC  
8321 Old Courthouse Rd. Suite 200  
Vienna, VA 22182-3817  
(703) 761-4100  
Customer No. 21254

### CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Amendment by facsimile with the United States Patent and Trademark Office to Examiner Quyen Phan Leung, Group Art Unit 2828 at fax number (703) 308-7724 this 17<sup>th</sup> day of April, 2002.

  
Sean M. McGinn  
Reg. No. 34,386

# 46,060

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

**The following new claims have been added:**

- 1     -- 21. A semiconductor laser diode chip with an active layer mounted on a substrate,  
2     comprising:
  - 3         a first pair of marks formed in the vicinity of said active layer and straddling said
  - 4         active layer; and
  - 5         a second pair of marks straddling said active layer, said second pair of marks located
  - 6         at a further distance from said active layer than said first pair of marks,
  - 7         wherein said second pair of marks align with a pair of substrate side marks formed at
  - 8         a position opposed to said second pair of marks.
  
- 1     22. The semiconductor laser diode chip, as claimed in claim 21, wherein said first pair of  
2     marks comprises thin lines formed parallel to said active layer.
  
- 1     23. The semiconductor laser diode chip, as claimed in claim 22, wherein said first pair of  
2     marks are formed by a metallic film.
  
- 1     24. The semiconductor laser diode chip, as claimed in claim 21, wherein said first pair of  
2     marks comprises lines formed on an upper portion of said active layer.
  
- 1     25. The semiconductor laser diode chip, as claimed in claim 24, wherein said lines have a  
2     same width as that of said active layer.
  
- 1     26. The semiconductor laser diode chip, as claimed in claim 21, wherein said second pair of  
2     marks have a circular shape.
  
- 1     27. The semiconductor laser diode chip, as claimed in claim 21, wherein said pair of  
2     substrate side marks have a diameter different than a diameter of said second pair of marks.

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1 28. The semiconductor laser diode chip, as claimed in claim 21, wherein a distance between  
2 each individual mark of said first pair of marks is 10  $\mu$ m.

1 29. An optical module, comprising:  
2 a substrate; and  
3 the semiconductor laser diode chip of claim 1 formed on the substrate.

1 30. The module of claim 29, further comprising:  
2 an optical fiber arranged on the substrate and connected to the semiconductor laser  
3 diode chip.

1 31. A semiconductor laser diode chip to be mounted on a substrate for an optical module,  
2 comprising:  
3 an active layer;  
4 a positioning-type mark in a vicinity of said active layer; and  
5 a measurement-type mark located between said active layer and said positioning-type  
6 mark.

1 32. The semiconductor laser diode chip as claimed in claim 31, wherein said chip is  
2 positioned on said substrate by aligning said position-type mark with a another position-type  
3 mark on said substrate.

1 33. The semiconductor laser diode chip as claimed in claim 32, wherein said chip is  
2 positioned on said substrate by measuring a distance between said active layer and said  
3 measurement-type mark. –